What is claimed is:

1. An integrated circuit comprising:

a peripheral interface to receive an interrupt request;

a memory interface to communicate with a memory device;

a processor interface to communicate with a processor; and

a logic circuit connected to the peripheral interface to acquire the interrupt information associated with the interrupt request, wherein the logic circuit is also connected to the processor interface and the memory interface to pass the interrupt information to the memory device without passing the interrupt information to the processor interface.

2. The integrated circuit of claim 1 further includes a memory unit to store the interrupt information before the interrupt information is passed to the memory interface.

3. The integrated circuit of claim 1 further comprising a configuration circuit to store configuration address indicating a location in the memory device to store the interrupt information.

4. The integrated circuit of claim 3, wherein the configuration circuit includes a read only memory device to store the configuration address.

5. The integrated circuit of claim 1 further comprising a graphics interface to communicate with a graphics card.

6. A system comprising:

a processor;

a memory device; and

a chipset connected to the processor and the memory device, wherein the chipset is configured to receive interrupt information and to pass the interrupt information to the memory device without notifying the processor the presence of the interrupt information.

7. The system of claim 6, wherein the chipset includes a graphic and memory control hub to process graphic and memory information and to provide access between the processor and the memory device.

8. The system of claim 7, wherein the chipset further includes an input output control hub connected to the graphic and memory control hub to process input output information between the chipset and external devices.

9. The system of claim 8, wherein the chipset further includes an interrupt controller to receive the interrupt information.

10. The system of claim 6, wherein the processor is configured to poll the memory device to check for the interrupt information at a time independent from a time the interrupt information is received by the chipset.

11. The system of claim 6 further comprising a second processor connected to the chipset.

12. The system of claim 11, wherein the second processor is configured to poll the memory device to check for the interrupt information at a time independent from a time the interrupt information is received by the chipset.

13. A method comprising:

receiving an interrupt request at an interrupt controller;

acquiring, at the interrupt controller, interrupt information corresponding to the interrupt request; and

passing the interrupt information from the interrupt controller to a memory device without passing the interrupt information to a processor.

14. The method of claim 13 further comprising:

polling the memory device to check for the interrupt information.

15. The method of claim 14, wherein polling is performed by the processor at a time independent from a time the interrupt request is received by the interrupt controller.

16. The method of claim 14 further comprising:

performing an interrupt function based on the interrupt information.

17. The method of claim 14, wherein polling is performed by a second processor a time independent from a time the interrupt request is received by the interrupt controller.

18. The method of claim 13, wherein the memory device and the interrupt controller are located in separate chips.

19. The method of claim 13, wherein passing the interrupt information from the interrupt controller to the memory device includes writing the interrupt information to the memory device at a memory location according to configuration information.

20. The method of claim 19, wherein the configuration information is stored in the interrupt controller.

21. A method comprising:

receiving an interrupt request at a chipset, the chipset connecting to a processor;

acquiring, at the chipset, interrupt information corresponding to the interrupt request;

storing the interrupt information at a memory location without notifying the processor the interrupt request; and

polling the memory device to check for the interrupt information, wherein polling is performed at a time independent from a time the interrupt request is received at the chipset.

22. The method of claim 21, wherein polling is performed by the processor.

23. The method of claim 21, wherein polling is performed by a second processor connected to the chipset.

24. The method of claim 21 further comprising:

performing an interrupt function based on the interrupt information stored in the memory location.

25. The method of claim 21, wherein storing the interrupt information at the memory location includes storing the interrupt information in a memory device separate from the processor and the chipset.

26. The method of claim 25, wherein storing the interrupt information at the memory location includes storing the interrupt information at the memory location according to a configuration information.

27. The method of claim 26, wherein the configuration information is stored in the chipset.